APPLICATION DATA SHEET

APPLICATION INFORMATION

Filing Date::	10-10-2003
Application Type::	Regular
Subject Matter::	Utility
Title::	Methods of Testing Interconnect Lines in Programmable Logic Devices Using Partial Reconfiguration
Attorney Docket Number::	X-1338 US
Request for Early Pub?::	No
Request for Non-Pub?::	Yes
Total Drawing Sheets::	09
Small Entity?::	No
Petition included?::	No

APPLICANT INFORMATION

Applicant Authority Type::	Inventor
Primary Citizenship Ctry::	US
Status::	Full Capacity
Given Name::	David
Family Name::	Mark
Street::	1724 Briarbush Court
City::	San Jose
State or Province::	California
Postal or Zip Code::	95131

Applicant Authority Type::	Inventor
Primary Citizenship Ctry::	US
Status::	Full Capacity
Given Name::	Randy
Middle Name::	J.
Family Name::	Simmons
Street::	1940 Huxley Court
City::	San Jose

State or Province:: California
Postal or Zip Code:: 95125

Applicant Authority Type:: Inventor
Primary Citizenship Ctry:: US
Status:: Full Capacity
Given Name:: Huy-Quang
Family Name:: Le
Street:: 1117 Foxhollow Court
City:: Milpitas
State or Province:: California
Postal or Zip Code:: 95035

Applicant Authority Type:: Inventor
Primary Citizenship Ctry:: Bangladesh
Status:: Full Capacity
Given Name:: Kazi
Middle Name:: S.
Family Name:: Afzal
Street:: 1103 Reed Avenue
City:: Sunnyvale
State or Province:: California
Postal or Zip Code:: 94086

CORRESPONDENCE INFORMATION

Correspondence Customer Number:: 24309

REPRESENTATIVE INFORMATION

Representative Customer Number::	**24309**	

ASSIGNEE INFORMATION

Assignee Name::	Xilinx, Inc.
Street::	2100 Logic Drive
City::	San Jose
State or Province::	California
Postal or Zip Code::	95124